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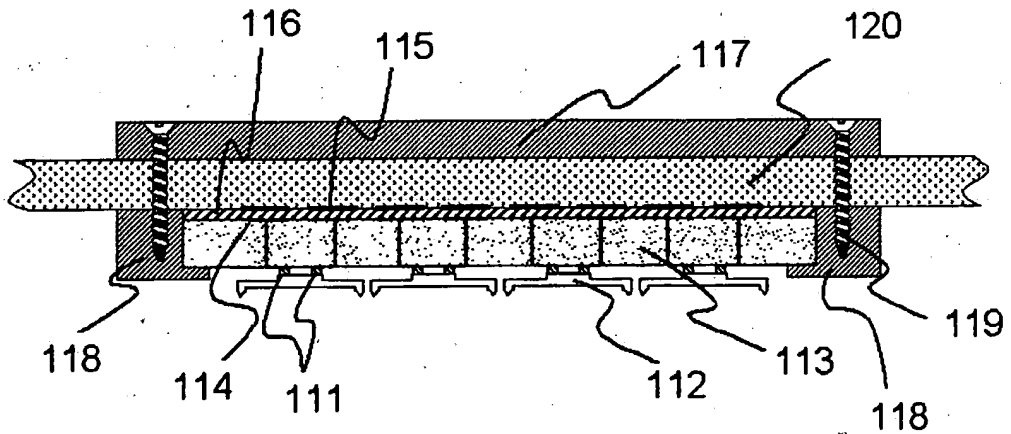

(57) Abstract: Disclosed is a probe card that comprises: a probe substrate including a plurality of probes and a support substrate for supporting the probes; a PCB having at least one probe substrate; and a space transformer having a first surface connected to the probe substrate and a second surface connected to the PCB, and adjusting gaps between the probe substrate and the PCB, wherein the probe comprises an elasticity unit including: a first terminal and connected to the support substrate; and a second terminal, the positions of which are elastically transformed and recovered upwards and downwards when pressure is applied or canceled; a contact unit protruding on a bottom portion of the second terminal of the elasticity unit; and a probe conductive pattern provided from the contact unit to the surface of the support substrate via the elasticity unit.

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Probe, Probe Card and Probe Manufacturing Method

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a probe for testing semiconductor integrated circuit (IC) devices formed on a semiconductor wafer, probe card on which a plurality of probes is installed, and probe manufacturing method.

(b) Description of the Related Art

In general, semiconductor IC devices are tested during or after manufacture, or during packaging, to match the total or partial electrical characteristics of the devices with those of original designs.

An instrument for the above-noted test is a probe instrument on which a tester and a probe card are installed, and the probe card electrically connects various electrical signal generators in the tester with pads in the semiconductor IC devices, or an electrical signal detector of the tester with the pads in the semiconductor IC devices.

Referring to FIGs. 1 to 3, a conventional probe and probe card will now be described.

FIGs. 1(a) and 1(b) show a prior tungsten needle probe card. As shown in FIG. 1(a), the needles 11 made of tungsten are provided in a predetermined array and are electrically insulated.

A tungsten needle jig 12 maintains the tungsten needles 11 in a high density, and a needle contact unit 13 is protruded from the tungsten needle jig 12. Another terminal unit 14 of the tungsten needles 11 is passed through a tungsten needle supporter 15 in low density and protrudes from the tungsten needle supporter 15. A connection unit (not illustrated) is connected to another terminal unit 14, passed through a circuit substrate 16, and electrically connected to a testing device (not illustrated.)

As shown in FIG. 1(b), when the tungsten needle jig 12 contacts the

needle contact unit 13 to pads 18 of a semiconductor IC device formed on a wafer 17, the testing device (not illustrated) is connected to an IC device through a tungsten needle probe card.

However, the conventional tungsten needle probe card having the above-described configuration reduces a pitch of the needle contact unit 13. Also, as many as the number of the needles is increased, it becomes difficult to array the needle contact unit 13 on an identical height, and a restriction of an expansion of the number of the needles 11 cannot fully satisfy the requirements of semiconductor manufacturers, who desire to increase the testing productivity by increasing the number of needles and concurrently testing many semiconductor devices. Also, the tungsten needles are manufactured by a sintering, and material defects such as cavities are densely provided to a contact unit that is acutely processed because of manufacturing features, and when they are repeatedly used, aluminum that is material of the pad of the semiconductor IC device is deposited on the defects and accordingly contact resistance is increased. To stably contact the needles 11 to the pad of the semiconductor IC, elasticity of the needle 11 is needed, but the tungsten needles lose their elasticity because the horizontal degree is distorted when they are repeatedly used. Also, the semiconductor IC tests are required at room temperature and high temperature, and since the probe and the probe card have different thermal expansion coefficients from the semiconductor IC wafer and also have different expansion directions when the temperature is increased, a sliding effect is generated between the contact unit of the probe and the pad of the semiconductor IC, and accordingly the contact resistance is increased and the contact states may be unstable. Also, when used for testing a high-speed semiconductor IC, since the lengths of the needles are long and the needles are adjacent to each other, the adjacent needles generate electrical interaction, and hence the precision of the test becomes unfavorable.

Another conventional thin film probe card will now be described. FIG. 2 shows a thin film probe card.

As shown, the conventional thin film probe card comprises a support plate 21, and a support film 22 is affixed on the support plate 21 by an elastomer layer

23. A conductive bumper 24 is provided on the support film 22 and optionally connected to a connection unit 25. The conductive bumper 24 is contacted to a pad 26 of the IC device, and a testing device (not illustrated) is connected to the IC device via the conventional thin film card.

The above-described thin film probe card generates problems because of its short stroke. In detail, it is possible to array the conductive bumper 24 up to a precise pitch and increase its precision, but the height of the conductive bumper becomes shorter than the diameter of the bottom portion of the bumper. That is, when the size of the bumper is minimized to array the bumper up to the precise pitch, its height is reduced and hence, dispersions of the height of the pad 26 of the semiconductor IC device cannot be fully accommodated, the contact problems between the conductive bumper 24 and the semiconductor IC pad 26 are generated.

Another conventional probe and probe card techniques related on a vertical operational probe assembly are disclosed in the US patent No. 5,134,365 and Korean patent 10-0212169. The vertical operational probes can increase the density, but other problems of the tungsten probes such as elasticity reduction generated by repeated use, difficulty for uniformly maintaining the height of the needle contact unit, and a problem of deposition of the pad material of the semiconductor IC on the contact unit. Also, the productivity is decreased since all the probes must be inserted into an auxiliary plate one by one.

The other conventional probe and probe card technique is disclosed in the Korean Laid Publication 2000-0017761 as shown in FIG. 3.

FIG. 3 shows a detail schematic diagram of a conventional probe and a probe card. A plurality of detailed probes 31 is provided on a glass substrate 32, the glass substrate 32 is affixed on an auxiliary circuit substrate 33, and the auxiliary circuit substrate 33 is combined with a main circuit board 35 via a buffer pad 34. A terminal of the probe 31 is electrically connected to the auxiliary circuit substrate 33 via a cavity on the glass substrate 32 using a wire 36, and the auxiliary circuit substrate 33 is electrically connected to the main circuit board 35 via the buffer pad 34 that includes a plurality of minute wires.

In general, the semiconductor ICs have different pad layouts according to their categories, and in order to test other categories of the semiconductor ICs when the conventional probe and probe card are used, the probe 31, the glass substrate 32 and the auxiliary circuit substrate 33 must be again manufactured except the main circuit board of the compatible probe card. Also, a space 37 for bonding the wire 36 is needed in addition to the probe 31, and in order to install a plurality of probes, wafers of large diameter must be used since the probes are processed after silicon wafer and glass wafer are bonded, and in this case, the product cost increases, the etching uniformity becomes poor and the characteristics of the respective probes are differentiated, and accordingly, the total quality of the probe card is worsened.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a probe card on which a plurality of probes is densely provided, the height of the probe being high enough to accommodate the dispersion of the height of the semiconductor IC pad, the height of the needle contact units being identical, variations of elasticity of the probes being rarely generated after their repeated use, and no cavity being generated to the probe contact unit.

It is another object of the present invention to provide a probe and a probe card of improved compatibility and productivity without using a glass substrate that is differently manufactured according to sizes and shapes of the semiconductor ICs.

It is still another object of the present invention to provide a high quality probe card of high integration and of less quality difference between the probes.

It is further another object of the present invention to provide a probe and a probe card for testing devices without variations of contact resistance at room temperature and high temperature and for minimizing interferences between the probes in testing a high-speed operational semiconductor IC so as to improve the reliability of test results.

It is still another object of the present invention to provide a probe and a probe card that can be used as a probe card for testing the semiconductor device wafer and as a socket for burn-in tests of LCD or semiconductor devices.

In one aspect of the present invention, a probe card comprises: a probe substrate including a plurality of probes and a support substrate for supporting the probes; a printed circuit board (PCB) having at least one probe substrate; and a space transformer having a first surface connected to the probe substrate and a second surface connected to the PCB, and adjusting gaps between the probe substrate and the PCB, wherein the probe comprises: an elasticity unit including: a first terminal and connected to the support substrate; and a second terminal, positions of which is elastically transformed and recovered upwards and downwards when pressure is applied or canceled; a contact unit protruded on a bottom portion of the second terminal of the elasticity unit; and a probe conductive pattern provided from the contact unit to the surface of the support substrate via the elasticity unit.

In another aspect of the present invention, a method for manufacturing a probe substrate comprises: performing a photo lithographic process on the top portion of a silicon wafer and generating a probe elasticity unit and a support substrate having a predetermined thickness; performing a photo lithographic process on the bottom portion of the silicon wafer and generating a probe contact unit; generating an insulation film on exposed silicon surfaces including the probe and the support substrate; and forming a probe conductive pattern that covers from the surface of the contact unit to the surface of the support substrate through the elasticity unit.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention:

FIG. 1(a) shows a conventional tungsten needle probe card;

FIG. 1(b) shows a contact state of a tungsten needle and a pad of a semiconductor IC when using the conventional tungsten needle probe card;

FIG. 2 shows an operation of a conventional thin film probe card;

FIG. 3 shows a conventional detailed probe and a probe card;

FIG. 4 shows a probe card according to a preferred embodiment of the present invention;

FIG. 5(a) shows a ground plan of a probe according to a first preferred embodiment of the present invention;

FIG. 5(b) shows a cross sectional view of FIG. 5(a) with respect to a line 1-1' ;

FIG. 5(c) shows a cross sectional view of FIG. 5(a) with respect to a line 2-2' ;

FIG. 5(d) shows an operation of the probe according to the first preferred embodiment of the present invention;

FIG. 6(a) shows a ground plan of a probe according to a second preferred embodiment of the present invention;

FIG. 6(b) shows a cross sectional view of FIG. 6(a) with respect to a line 1-1' ;

FIG. 6(c) shows a cross sectional view of FIG. 6(a) with respect to a line 2-2' ;

FIGs. 7(a) to 7(f) show processes for manufacturing the probe according to the first preferred embodiment of the present invention;

FIGs. 8(a) to 8(f) show processes for manufacturing the probe according to the second preferred embodiment of the present invention;

FIG. 9 shows a cross sectional view of a probe card including a conventional space transformer;

FIG. 10 shows a space transformer according to the first preferred embodiment of the present invention;

FIGs. 11(a) to 11(e) show processes for manufacturing the space transformer according to the first preferred embodiment of the present invention;

FIGs. 12(a) to 12(b) show processes for manufacturing the space

transformer according to the second preferred embodiment of the present invention;

FIG. 13 shows a space transformer according to third preferred embodiment of the present invention;

FIGs. 14(a) to 14(e) show processes for manufacturing the space transformer according to the third preferred embodiment of the present invention; and

FIGs. 15(a) and 15(b) show processes for manufacturing a micro solder ball in the probe card according to the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description, only the preferred embodiment of the invention has been shown and described, simply by way of illustration of the best mode contemplated by the inventor(s) of carrying out the invention. As will be realized, the invention is capable of modification in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

FIG. 4 shows a cross sectional view of a probe card according to a preferred embodiment of the present invention. As shown, the probe card comprises: a probe substrate 112 for including a plurality of probes and a support substrate for supporting the probes; a printed circuit board (PCB) 120 for installing at least one probe substrate 112; and a space transformer 113 for having a first surface contacted with the probe substrate 112 and a second surface contacted with the PCB 120 and controlling a gap between the probe substrate 112 and the PCB 120.

The probe comprises a first terminal and a second terminal. The first terminal is connected to the support substrate, and the second terminal comprises an elasticity unit, positions of which are elastically transformed and recovered upwards and downwards when pressure is applied or canceled; a contact unit

protruded on a bottom portion of the elasticity unit; a probe conductive pattern provided from the contact unit to the surface of the support substrate via the elasticity unit; first and second metallic housings 117 and 118 formed from an outer portion of the space transformer 113 to a top portion of the PCB 120; and a screw 119.

Referring to FIG. 4, components and manufacturing method of the probe card will now be described.

The probe according to the first preferred embodiment will be described. FIG. 5(a) shows a ground plan of a probe, FIG. 5(b) shows a cross sectional view of FIG. 5(a) with respect to a line 1-1' , FIG. 5(c) shows a cross sectional view of FIG. 5(a) with respect to a line 2-2' , and FIG. 5(d) shows an operation of the probe.

As shown, the probe 41 is formed by optionally etching a predetermined portion of a single or poly crystalline wafer, and the probes are separated from a peripheral probe substrate 43 except one or a plurality of connection units 42. A contact unit 44 is formed to protrude higher than other peripheral units. The surface of the probe and the probe substrate are formed of an insulation film 45. Probe metal 47 that covers a predetermined bottom portion of the probe 41 including the protruded contact unit 44 and covers the top portion of the probe 41 and a probe pad 46 that is formed to connect with an external PCB (not illustrated) are formed to be connected with each other by plating them with solid metal or alloy, and accordingly, the contact unit 44 and the probe pad 46 are electrically connected.

FIG. 5(d) shows a state that a predetermined pressure is supplied to the probe 41 and the probe 41 is contacted to a pad 49 of a semiconductor IC device 48.

FIG. 6(a) shows a ground plan of a probe according to a second preferred embodiment of the present invention, FIG. 6(b) shows a cross sectional view of FIG. 6(a) with respect to a line 1-1' , and FIG. 6(c) shows a cross sectional view of FIG. 6(a) with respect to a line 2-2' .

As shown, the probe 51 is formed by optionally etching a predetermined

portion of a single or poly crystalline wafer, and the probes are separated from a peripheral probe substrate 53 except one or a plurality of connection units 52. A contact unit 54 is formed to be protruded higher than other peripheral units. A circular or polygonal groove 55 that penetrates a wafer is formed on the wafer. The diameter of the groove 55 can be from several micrometers to several hundreds of micrometers, and if considering a subsequent plating process, several micrometers are appropriate.

All the silicon surfaces including the probe, the probe substrate and the groove are formed of insulation film 56. Probe metal 58 that covers the protruded contact unit, the bottom portion of the probe, the groove and inner walls of the groove 55 and a pad 57 that is formed on the top portion of the substrate to connect with an external PCB (not illustrated) are formed to be connected with each other by plating them with solid metal or alloy, and accordingly, the contact unit 54 and the pad 57 are electrically connected.

It is known that the single or poly crystalline silicon is of high elasticity, its plasticity transformation is rarely generated, and its intensity in the case of a minute structure of micrometers is greater than the stainless steel. Also, since the probe according to the present invention is made of the above-noted crystalline silicon, the original form is preserved without any distortion or plasticity transformation even when the probe is repeatedly contacted hundreds of times.

A method for manufacturing the probe according to the first and second preferred embodiments will now be described.

The first step is to adjust the thickness of the probe and obtain a top space. As shown in FIG. 7(a), thin film for etching the silicon, such as silicon nitride film, silicon oxide film or their compound film is formed on the top portion of the single or poly crystalline silicon wafer 61 as a protection film 62, and a photoresist pattern is formed thereon via a photo process. After this, a predetermined pattern is formed on the protection film 62 by using a dry etching that uses phosphoric acid or a wet etching that uses CCl_2F_3 in the case of the nitride film or by using the wet etching that uses HF or the dry etching that uses gases such as CCl_2F_3, CF_4, C_2F_6 and C_3F_8 in the case of the oxide film.

As shown in FIG. 7(b), the silicon on the bottom portion is etched at a predetermined depth using the protection film 62 and the protection film is uncovered.

As to the above-described silicon etching, when the single crystalline wafer is used, characteristics that etching speeds of KOH, Ethylene Diamine Pyrocathechol (EDP) and TetraMethyl Ammonium Hydroxide (TMAH) according to crystal directions of the silicon 111 are slow about several thousand times of the etching speeds of other crystal directions are used to perform an anisotropic wet etching or an anisotropic dry etching that uses gases such as Cl_2, CCl_4, BCl_3, $CHCl_3$, CHF_3 and CF_4, and when the poly crystalline wafer is used, an anisotropic etching using the dry etching is performed. In this instance, the depth of the wafer to be etched is appropriately selected according to the thickness of the wafer, the thickness of the desired probe and the height of a contact needle unit of the probe. Here, the thickness of the probe is very important since the thickness as well as the width and length of the probe is a variable that determines the elasticity and intensity of the probe when the pressure for the contact is supplied, and therefore, an accurately calculated thickness must be formed according to usage environments of the desired probe, and since the usage environments can be greatly varied, detailed thickness will not be provided in the present invention.

The second step is to form an appearance of the probe. As shown in FIG. 7(c), an outer shape unit 63 of the probe is etched via the above-noted anisotropic etching so that the outer shape unit 63 is penetrated onto the bottom portion or a predetermined portion of the silicon film 64 is remained. In this instance, in the case a vacuous adsorption device is used in a subsequent process, it is easy to set aside the silicon film 64. Also, the thickness of the remaining silicon must be slimmer than the height of the probe' s contact unit to be formed in the subsequent step so that the remaining film is removed when the probe' s contact unit is formed and accordingly, the outer shape of the probe is completed.

The third step is to from the contact unit of the probe. As shown in FIG. 7(d), portions except a contact unit 65 on the bottom portion of a probe substrate are removed as high as the height of the contact unit via the photo process and

the etching process used when forming the photoresist pattern. Accordingly, the shape of the probe including the contact unit is completed.

In this instance, so as to process the end portion of the contact unit 65 in the shape of a pyramid or a similar sharp shape, an isotropic dry or wet etching that uses gas such as X_eF_2 is used, and when using the single crystalline wafer, the crystal directions are appropriately provided, the anisotropic wet etching is used.

The fourth step is to electrically insulate the manufactured probes. As shown in FIG. 7(e), insulation film 66 such as the silicon nitride film or the silicon oxide film is provided for a full insulation on all the surfaces of the probe that is provided on the bottom portion of the probe substrate via the photo process and the etching process and the surfaces of the substrate.

Physical or chemical vapor deposition is possible to form the thin film, if considering the product cost or the film quality, the thermal oxide film forming method using an electrical furnace is the most appropriate method. In this instance, the appropriate thickness of the insulation thin film ranges from several hundreds to several ten thousand angstroms.

The fifth step is to electrically connect a pad 67 connected to the external PCB with a contact unit 68 of the probe. As shown in FIG. 7(f), the contact unit 68 and a predetermined portion of the probe are optionally plated using the metal of good conductivity, oxidation-resistance and relative high hardness such as nickel, tungsten and chrome or the alloy 69 via the photo process and the thin film forming process, and the top portion of the probe and the top portion of the probe substrate connected to it are optionally plated in a pad shape of several ten to several hundred micrometers using the above-noted metal and the alloy 69 via the photo process and the thin film forming method. Accordingly, when the contact unit 68 and the pad 67 of the probe are electrically connected, the silicon probe and the probe substrate are formed.

The pad 67 is directly joined with a micro solder ball that will be described in a subsequent step, and it is good to form an under bumper metallurgy (UBM) unit 70 on the pad 67 for a stable solder ball junction.

The UBM unit 70 that comprises a diffusion protecting film for protecting

the diffusion of the solder and a wet film such as the gold or the copper for improving the wetness of the solder is optionally formed via the photo process and a conventional electrolyte or electroless plating method.

Next, a process for manufacturing the probe according to the second preferred embodiment will be described.

FIGs. 8(a) to 8(f) show processes for manufacturing the probe according to the second preferred embodiment of the present invention.

The probe manufacturing method according to the second preferred embodiment is identical with that according to the first preferred embodiment except that a penetration hole is concurrently manufactured, and the metallic wiring for electrically connecting the contact unit with the pad of the probe is formed on the bottom portion of the probe in the step of forming the appearance of the probe.

As shown in FIG. 8(a), the thickness of the probe is adjusted and a space for bending the probe is obtained. First, a thin film for etching the silicon, such as silicon nitride film, silicon oxide film or their compound film is formed on the top portion of the single or poly crystalline silicon wafer 1001 as a protection film 1002, and a photoresist pattern is formed thereon via a photo process. After this, a predetermined pattern is formed on the protection film 1002 by using a dry etching that uses phosphoric acid or a wet etching that uses CCl_2F_3 in the case of the nitride film or by using the wet etching that uses HF or the dry etching that uses gases such as CCl_2F_3, CF_4, C_2F_6 and C_3F_8 in the case of the oxide film.

As shown in FIG. 8(b), the silicon on the bottom portion is etched at a predetermined depth using the protection film 1002 and the protection film is uncovered. As to the above-described silicon etching, when the single crystalline wafer is used, characteristics that etching speeds of KOH, Ethylene Diamine Pyrocathechol (EDP) and TetraMethyl Ammonium Hydroxide (TMAH) according to crystal directions of the silicon 111 are slow about several times of the etching speeds of other crystal directions are used to perform an anisotropic wet etching or an anisotropic dry etching that uses gases such as Cl_2, CCl_4, BCl_3, $CHCl_3$, CHF_3 and CF_4, and when the poly crystalline wafer is used, an anisotropic etching using the dry etching is performed.

Next, as shown in FIG. 8(c), an appearance of the probe and a penetration hole are formed. An outer shape unit 1003 of the probe and the penetration hole 1004 are etched using the anisotropic etching, and accordingly, they are penetrated to the bottom of the silicon wafer 1001 or a predetermined amount of a silicon film 1005 is preserved.

In this instance, in the case a vacuous adsorption device is used in a subsequent process, it is easy to set aside the silicon film. Also, the thickness of the remained silicon must be slimmer than the height of the probe' s contact unit to be formed in the subsequent step so that the remained film is removed when the probe' s contact unit is formed and accordingly, the outer shape of the probe is completed.

As shown in FIG. 8(d), portions except a contact unit 1006 on the bottom portion of a probe substrate are removed as high as the height of the contact unit via the photo process and the etching process. Accordingly, the shape of the probe including the contact unit is completed. In this instance, so as to process the end portion of the contact unit 1006 in the shape of a pyramid or a similar sharp shape, an isotropic dry or wet etching that uses gas such as X_eF_2 is used, and when using the single crystalline wafer, the crystal directions are appropriately provided, the anisotropic wet etching is used.

The next step is to electrically insulate the manufactured probes. As shown in FIG. 8(e), insulation film 1007 such as the silicon nitride film or the silicon oxide film is provided on all the surfaces of the probe and the surfaces of the substrate for a full insulation.

Physical or chemical vapor deposition is possible to form the thin film; if considering the product cost or the film quality, the thermal oxide film forming method using an electrical furnace is the most appropriate method. In this instance, the appropriate thickness of the insulation thin film ranges from several hundreds to several ten thousand angstroms.

Next, a pad 1008 connected to the external PCB is electrically connected with a contact unit 1009 of the probe. As shown in FIG. 8(f), first, areas from the junction unit to an adjacent region of the penetration hole are connected and a

predetermined portion of the probe is optionally plated using the metal of good conductivity, oxidation-resistance and relative high hardness such as nickel, tungsten and chrome or the alloy 1010 via the photo process and the thin film forming process, and the top portion of the probe and the top portion of the probe substrate connected to it are optionally plated in a pad shape of several ten to several hundred micrometers using the above-noted metal and the alloy 1010 via the photo process and the thin film forming method. Accordingly, when the contact unit 1009 and the pad 1008 of the probe are electrically connected, the silicon probe and the probe substrate are formed.

In this instance, the physical vapor deposition (PVD), the chemical vapor deposition (CVD), the electrolyte plating or the electroless plating is used to form the thin film of the metal or the alloy, and particularly, the CVD, the electrolyte plating or the electroless plating is effectively used to perform fluent electrical connections between the top and bottom following the side wall of the penetration hole.

The pad 1008 of the probe is directly joined with a micro solder ball that will be described in a subsequent step, and it is good to form an under bumper metallurgy (UBM) unit 1011 on the pad 1008 for a stable solder ball junction.

The UBM unit 1011 that comprises a diffusion protecting film for protecting the diffusion of the solder and a wet film such as the gold or the copper for improving the wetness of the solder is optionally formed via the photo process and a conventional electrolyte or electroless plating method.

The steps of the above-described processes can be changed or modified, and it is obvious that the changes or the modifications are matched with the preferred embodiment wherein a silicon wafer is used, a predetermined portion of the wafer forms a probe, and a probe pad for a connection with a PCB is formed on the probe.

A space transformer will now be described with reference to drawings.

FIG. 9 shows a cross sectional view of a conventional probe card including a space transformer. The probe card comprises a main board 71; a space transformer 72; a probe 73; and housings 74 and 75. These parts are combined

using screws 76.

In the above-described probe card, a user appropriately determines and uses a distance ' a' between a bottom surface of the main board 71 and a probe contact unit 73 or a distance ' b' between a top surface of the main board 71 and the probe contact unit 73 according to specifications of peripheral devices that use the probe card such as a probe machine or a testing device. That is, the distances ' a' and ' b' must be adjusted and manufactured according to the user' s desired specifications since the probe card is one of compatible expendable supplies. The thickness of the probe card is adjusted by the space transformer 72 that maintains electrical connections and appropriately adjusts the total thickness of the probe card.

Conventional PCBs of FR_4 or polyimide are widely used for the space transformer, but when considering thermal and mechanical transformation generated by iterated use of the probe card and the thermal transformations generated at the time of a micro solder ball junction, the ceramic space transformer is the best choice.

Therefore, in the present invention, the ceramic space transformer will be used for subsequent preferred embodiments.

Referring to FIG. 10, the structure of the space transformer according to the first preferred embodiment will now be described.

As shown, the space transformer comprises a ceramic substrate 81 including a penetration hole 82 having a predetermined size and a predetermined thickness and being positioned on a predetermined location; a penetration hole conductive unit formed in the penetration hole 82; first and second conductive patterns 84 and 88 each of which formed on both surfaces of the ceramic substrate 81 and connected via the penetration hole conductive unit; and a photoresist film 85 for covering and protecting a predetermined portion of the first conductive pattern 84.

Referring to FIGs. 11(a) to 11(e), a process for manufacturing the space transformer according to the first preferred embodiment will now be described.

As shown in FIG. 11(a), the ceramic substrate 81 is processed according

to a predetermined size and thickness, and as shown in FIG. 11(b), a penetration hole 82 with a diameter of a several hundreds of micrometers is generated on a predetermined position of the ceramic substrate 81. A method for generating the penetration hole 82 will be described later.

As shown in FIG. 11(c), all the surfaces of the ceramic substrate 81 are plated with metal or alloy using electrolyte or electroless plating so as to form a plating film 83, and as shown in FIG. 11(d), both top and bottom surfaces of the ceramic substrate are mechanically processed to remove the plating film, and accordingly, the plating film is preserved only in the penetration hole.

As shown in FIG. 11(e), the desired electrical circuits are printed on both surfaces of the ceramic substrate via a screen printing method by using conductive pastes, or the desired first and second conductive patterns 84 and 88 are formed on both surfaces of the ceramic substrate via a lift-off method that performs a physical vapor deposition to deposit a conductive film on the photoresist pattern and remove the photoresist to obtain the desired patterns or via a method for depositing a conductive film and etching by using a photoresist pattern.

When a micro solder ball is joined to the first conductive pattern 84, the first conductive pattern 84 functions as a solder ball junction pad 86 to which the micro solder ball is joined and as a wire pattern for electrically connecting the solder ball junction pad 86 with the penetration hole 82, and the second conductive pattern 88 functions as a conductive pattern for electrical connection with the substrate.

Next, as shown in FIG. 10, a photoresist film 85 for protecting the conductive patterns is coated on the junction surface of the micro solder ball, and a conductive layer of the solder ball junction pad 86 to which the micro solder ball is joined is exposed via the photo process.

After this, a UBM unit 87 for a stable junction at the time of the micro solder ball junction is formed on the exposed conductive layer. The UBM unit 70 that comprises a diffusion protecting film (i.e., nickel) for protecting the diffusion of the solder and a wet film (i.e., the gold or the copper) for improving the wetness of the solder is optionally formed via a conventional electrolyte or electroless

plating method.

Referring to FIGs. 12(a) and 12(b), a process for manufacturing the space transformer according to a second preferred embodiment of the present invention will now be described.

As shown in FIG. 12(a), a pattern 89 such as a resist is formed via the photo process so that a wiring pattern may be formed on both surfaces of the ceramic substrate 81 through which the penetration hole 82 is generated, and then the plating film 83 is formed on portions where the resist is not coated by the electrolyte or electroless plating method. After this, when the resist film is removed, the desired wiring can be formed as the plating film 83.

Since the processes of forming the protection film and the UBM unit are identical with those for manufacturing the space transformer according to the first preferred embodiment, no further description will be provided.

Here, the penetration hole will be described.

In general, it is very difficult to bore a fine penetration hole through a thick ceramic substrate. Therefore, a wheel tool coated with diamonds is used to bore the penetration hole having a diameter of several hundreds of micrometers on the ceramic substrate. In this instance, when the thickness of the ceramic substrate is about 1 to 2mm, the penetration hole having the diameter of several hundred micrometers can be relatively easily bored, but when the thickness is greater than 3mm, or 5 to 6mm, the boring process is very difficult and the corresponding cost is greatly increased.

Hence, to solve this problem, ceramic compounds that are not sintered are adsorbed to a paper and a hole is bored through the paper, and many sheets of the compounds are overlapped and sintered, and finally, a ceramic substrate having a desired thickness and on which the fine penetration hole is formed is obtained. However, the above-described method also has demerits in that it is very difficult to accurately predict the volume shrinkage generated by the sintering and modify the shrinkage and to precisely overlap the fine holes. Hence, a space transformer according to a third preferred embodiment for solving the above-described problem will now be described.

FIG. 13 shows a space transformer according to third preferred embodiment of the present invention. As shown, the space transformer comprises: a first ceramic substrate 91 having a plurality of first penetration holes 92; a first penetration hole conductive unit formed in the first penetration hole 92; a first conductive pattern 93 formed on both surfaces of the first ceramic substrate; a second conductive pattern 96 formed on both surfaces of the first ceramic substrate and connected to the first conductive pattern 93 via the first penetration hole conductive unit; a second ceramic substrate 91' having a plurality of second penetration holes 92' ; a second penetration hole conductive unit formed in the second penetration hole 92' ; a third conductive pattern formed on both surfaces of the second ceramic substrate 91' ; a fourth conductive pattern formed on both surfaces of the second ceramic substrate and connected to the third conductive pattern via the second penetration hole conductive unit; and an anisotropic conducting film 98 formed between the first and the second ceramic substrates 91 and 91' and electrically connecting the second and third conductive patterns.

Referring to FIGs. 14(a) to 14(e), processes for manufacturing the space transformer according to the third preferred embodiment of the present invention will be described.

As shown in FIG. 14(a), a plurality of ceramic substrates is processed with the thickness of 1 to 2mm so as to easily bore the fine penetration holes, and as shown in FIG. 14(b), the penetration holes 92 and 92' are bored through the processed first and second ceramic substrates 91 and 91' according to the above-described method.

As shown in FIG. 14(c), a pad 94 and a UBM unit 95 for joining the micro solder ball with a conductive thin film 93 are formed on one surface of the first ceramic substrate 91, and a conductive pad 96 for joining with the substrate is formed on another surface of the first ceramic substrate 91 according to the method identical with those of the first and second preferred embodiments as shown in FIG. 10 and FIG. 12(a). After this, conductive pads 97 are formed on both surfaces of the second ceramic substrate 91' as shown in FIG. 14(d).

Next, as shown in FIG. 14(e), the conductive pad 96 of the first ceramic

substrate 91 is matched with the conductive pad 97 of the second ceramic substrate 91' while an anisotropic conductive film 98 is positioned between the ceramic substrates 91 and 91' .

As to the anisotropic conductive film 98, conductive balls 99 are provided in an adhesive film, and when the both substrates are compressed at high temperature, electrical connection is allowed in the compression direction via the conductive balls 99.

Next, when the two ceramic substrates 91 and 91' are compressed at high temperature, they are combined, electrical connection is allowed between them, and they function as a single thick ceramic substrate.

An appropriate compression temperature in this case ranges from 50 to 300°C, and more accurate temperatures and compression pressures are determined according to categories of the anisotropic conductive film.

According to the above-described method, when two or more ceramic substrates, the thickness of which are appropriately adjusted, are combined, the space transformer of a desired thickness can be manufactured.

Next, referring to FIGs. 15(a) and 15(b), a process for mechanically and electrically combining the space transformer, the probe and the probe substrate will now be described.

As shown in FIG. 15(a), when micro solder balls 102 are individually bumped on the portions where the UBM units of the space transformer 101 are formed or the micro solder balls 102 are printed using solder pastes via a screen mask, the micro solder balls are formed.

As shown in FIG. 15(b), a silicon probe substrate 193 is provided on the micro solder balls on the space transformer and is then affixed on the same using a volatile adhesive, and a reflow process is performed at a temperature higher than the melting point of the micro solder balls 102 so as to volatilize the adhesive, and hence, the mechanical and electrical combination only by the micro solder balls 102 is completed. In this instance, the appropriate temperature of the reflow process ranges from 200 to 500°C, and the accurate temperature is differently determined according to the material of the solders to be utilized.

In the above, when the micro solder balls are used to combine the silicon probe substrate with the space transformer, it is only required that the size of the space transformer is to be matched with the specification of the probe card. That is, even when the silicon probe substrate includes a plurality of small modules and the small modules are repeatedly combined and are then combined with the space transformer, their effect is identical to that when a large silicon probe substrate is used according to the characteristics of the micro solder ball process. Accordingly, it is possible to manufacture a probe card that includes a plurality of probes without using a wafer of wide diameter when manufacturing the silicon probe substrate, and therefore, an expensive tool for processing the wafers of wide diameters is not needed, and a processing precision of the silicon probe substrate can be relatively increased. Also, damaged probes can be repaired more cheaply.

While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

According to the present invention, since fine probes are provided on a probe substrate via the photo process and the etching process, the density of the probes can be increased, and the heights of the needle contact unit of all the probes are uniformly maintained.

The probes manufactured according to the present invention preserve their high elasticity and their shapes are not transformed after their repeated uses, and the probe card makes it possible to concurrently test a plurality of semiconductor ICs.

Also, since the quality of the material used for the probes and the probe substrate is identical with that of the semiconductor IC substrate, the thermal expansion coefficient of the probe substrate according to the heat increase is identical with that of the semiconductor IC substrate, and since the configuration or shape of the probe substrate is similar to that of the semiconductor IC substrate and the expansion or shrinkage direction of the probe substrate generated

according to temperature variations is identical with that of the semiconductor IC substrate, the contact unit between the probe and the semiconductor IC pad is not slid at the time of a test when the temperature is increased and a stable connection is obtained.

Since the probe and the probe card according to the present invention have a shorter electrical path, electrical interferences of the adjacent probes are minimized, and thereby, test results of high reliability can be achieved when testing the high-speed operational semiconductor ICs.

Further, since the thickness of the probe card is adjusted using the ceramic space transformer, problems such as thermal and mechanical transformation generated by the iterated use of the probe card, and the thermal transformation in the case of the micro solder ball junction can be prevented.

By using the micro solder balls according to the present invention, the probe cards that have a plurality of probes can be manufactured without using the wafers of wide diameters when manufacturing the silicon probe substrate.

Also, probe cards for testing the semiconductor device wafers and sockets for the burn-in tests of the LCD and the semiconductor devices can be manufactured by a slight modification or a substitute of an additional auxiliary device.

WHAT IS CLAIMED IS:

1. A probe card comprising:

a probe substrate including a plurality of probes and a support substrate for supporting the probes;

a printed circuit board (PCB) having at least one probe substrate; and

a space transformer having a first surface connected to the probe substrate and a second surface connected to the PCB, and adjusting gaps between the probe substrate and the PCB,

wherein the probe comprises an elasticity unit including: a first terminal and connected to the support substrate; and a second terminal, positions of which is elastically transformed and recovered upwards and downwards when pressure is applied or canceled; a contact unit protruded on a bottom portion of the second terminal of the elasticity unit; and a probe conductive pattern provided from the contact unit to the surface of the support substrate via the elasticity unit.

2. The probe card of claim 1, wherein the prove card further comprises:

an anisotropic conductive film formed between the PCB and the space transformer; and

a micro solder ball, formed between the space transformer and the probe substrate, for electrically and mechanically combining the space transformer and the probe substrate.

3. The probe card of claim 1, wherein the probe card further comprises an under bumper metallurgy (UBM) unit formed on a first conductive pad of the space transformer.

4. The probe of claim 1, wherein the probe card further comprises a housing formed from a top portion of the PCB to an outer portion of the space transformer.

5. The probe card of claim 1, wherein the space transformer comprises:

a ceramic substrate processed with a predetermined size and thickness and including a penetration hole generated on a predetermined position and having a predetermined size;

a penetration hole conductive unit formed in the penetration hole;

first and second conductive patterns respectively formed on both surfaces of the ceramic substrate and connected to each other via the penetration hole conductive unit; and

a photoresist film for covering and protecting a predetermined portion of the first conductive pattern.

6. The probe card of claim 1, wherein the space transformer comprises:

a first ceramic substrate having a plurality of first penetration holes;

a first penetration hole conductive unit formed in the first penetration hole;

first and second conductive patterns respectively formed on both surfaces of the first ceramic substrate and connected to each other via the first penetration hole conductive unit;

a second ceramic substrate having a plurality of second penetration holes;

a second penetration hole conductive unit formed in the second penetration hole;

third and fourth conductive patterns respectively formed on both surfaces of the second ceramic substrate and connected to each other via the second penetration hole conductive unit; and

an anisotropic conductive film formed between the first and second ceramic substrates and mechanically and electrically connecting the second conductive pattern with the third conductive pattern.

7. A probe substrate comprising:

a support substrate;

an elasticity unit including: a first terminal and connected to the support substrate; and a second terminal, positions of which is elastically transformed and recovered upwards and downwards when pressure is applied or canceled;

a contact unit protruded on a bottom portion of the second terminal of the elasticity unit; and

a probe conductive pattern provided from the contact unit to the surface of the support substrate via the elasticity unit.

8. The probe substrate of claim 7, wherein the support substrate, the elasticity unit and the contact unit are made of single or poly crystal silicon.

9. The probe substrate of claim 7, wherein the probe substrate comprises: a penetration hole that bores the support substrate from top to bottom and has a predetermined diameter; and a probe pad that is a predetermined portion of the probe conductive pattern and is formed on the top surface of the support substrate, and the probe conductive pattern reaches to the probe pad from the contact unit via the penetration hole.

10. A space transformer comprising:

a ceramic substrate processed with a predetermined size and thickness and including a penetration hole generated on a predetermined position and having a predetermined size;

a penetration hole conductive unit formed in the penetration hole;

first and second conductive patterns respectively formed on both surfaces of the ceramic substrate and connected to each other via the penetration hole conductive unit; and

a photoresist film for covering and protecting a predetermined portion of the first conductive pattern.

11. The space transformer of claim 10, wherein the space transformer further comprises an under bumper metallurgy (UBM) unit formed on the first conductive pad.

12. A space transformer comprising:

a first ceramic substrate having a plurality of first penetration holes;

a first penetration hole conductive unit formed in the first penetration hole;

first and second conductive patterns respectively formed on both surfaces of the first ceramic substrate and connected to each other via the first penetration hole conductive unit;

a second ceramic substrate having a plurality of second penetration holes;

a second penetration hole conductive unit formed in the second penetration hole;

third and fourth conductive patterns respectively formed on both surfaces of the second ceramic substrate and connected to each other via the second penetration hole conductive unit; and

an anisotropic conductive film formed between the first and second ceramic substrates and mechanically and electrically connecting the second conductive pattern with the third conductive pattern.

13. The space transformer of claim 12, wherein the space transformer further comprises:

a photoresist film for covering and protecting a predetermined portion of the first conductive pattern; and

an under bumper metallurgy (UBM) unit formed on the first conductive pad.

14. The space transformer of claim 12, wherein the thickness of the first and second ceramic substrates ranges from 1 to 2mm.

15. A method for manufacturing a probe substrate comprising:

(1) performing a photo lithographic process on the top portion of a silicon wafer and generating a probe elasticity unit and a support substrate having a predetermined thickness;

(2) performing a photo lithographic process on the bottom portion of the silicon wafer and generating a probe contact unit;

(3) generating an insulation film on exposed silicon surfaces including the probe and the support substrate; and

(4) forming a probe conductive pattern that covers from the surface of the contact unit to the surface of the support substrate through the elasticity unit.

16. The method of claim 15, wherein a penetration hole that penetrates the support substrate from top to bottom is provided on the silicon wafer in (1).

17. The method of claim 15, wherein a metal or an alloy is optionally plated in (4).

18. A method for manufacturing a space transformer comprising:

(a) forming a penetration hole having a predetermined size and a predetermined thickness on a ceramic substrate;

(b) forming a plating film on the wall of the penetration hole;

(c) forming a conductive pattern on both surfaces of the ceramic substrate;

(d) forming a photoresist pattern that covers a predetermined portion of the conductive pattern and protects the pattern; and

(5) forming an under bumper metallurgy (UBM) unit on the exposed conductive pattern.

19. The method of claim 18, wherein an electrical circuit is provided on both surfaces of the ceramic substrate using conductive pastes via a screen printing method in (b).

20. The method of claim 18, wherein a conductive film is provided on the photoresist pattern via a physical vapor deposition, and a predetermined portion of the photoresist is removed to lift off a desired pattern in (b).

21. The method of claim 18, wherein a conductive film is provided on the photoresist pattern via a physical vapor deposition and a photo lithographic process is performed in (b).

FIG.1A

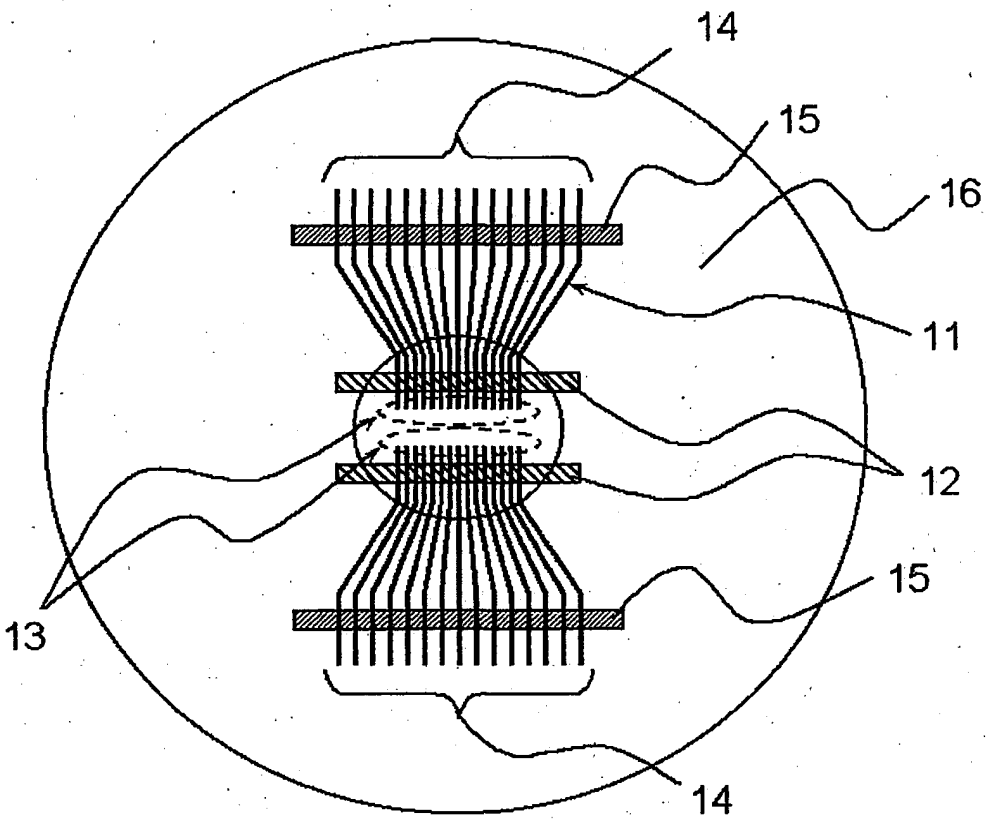

FIG.1B

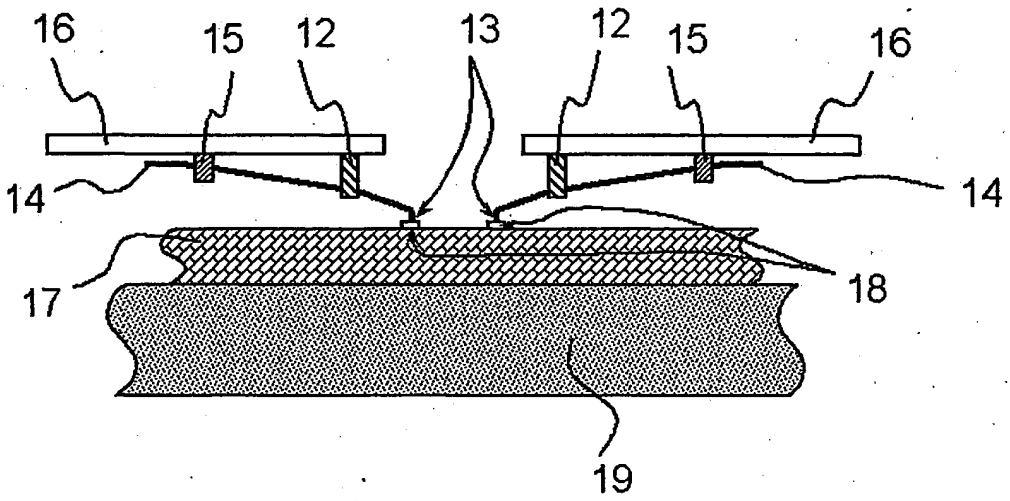

FIG.2

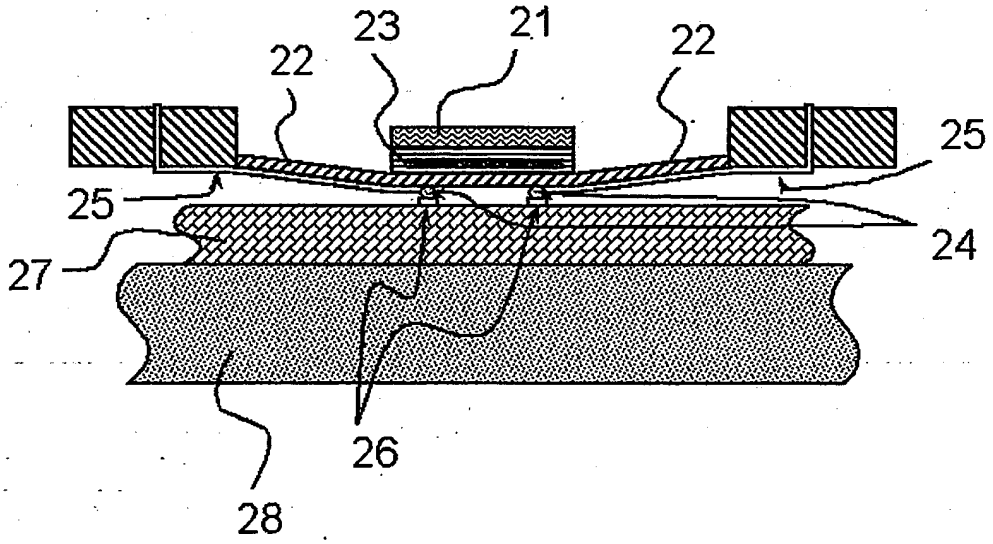

FIG.3

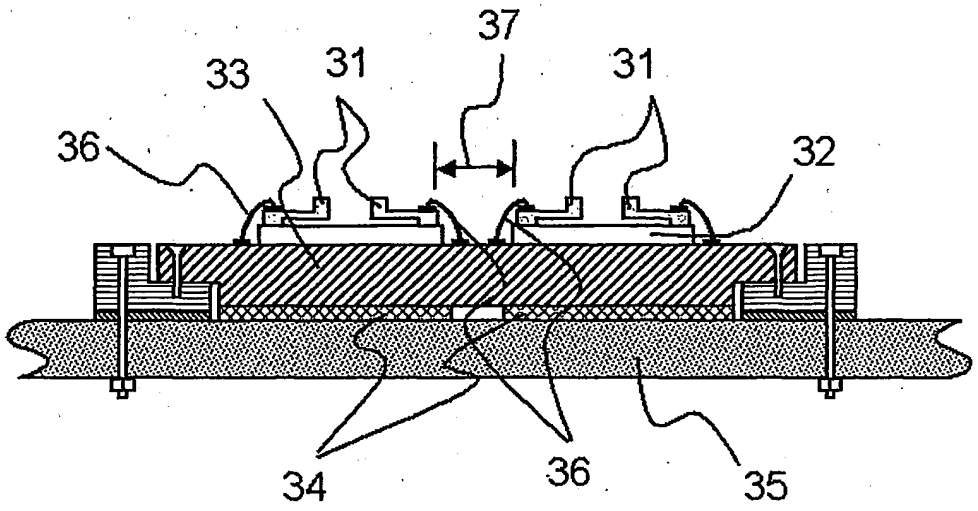
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FIG.4

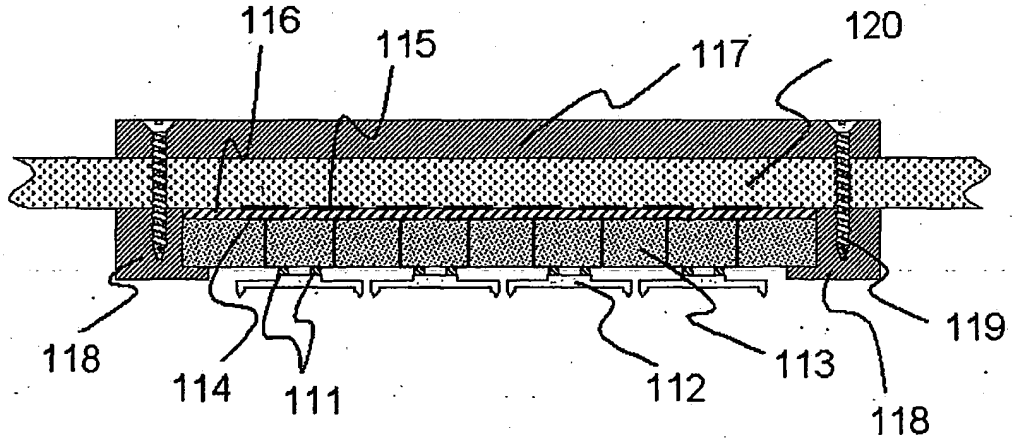
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FIG.5A

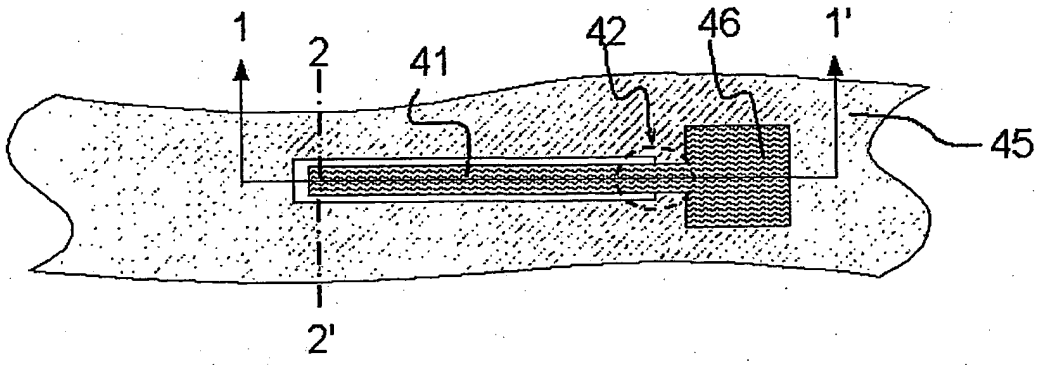


FIG.5B

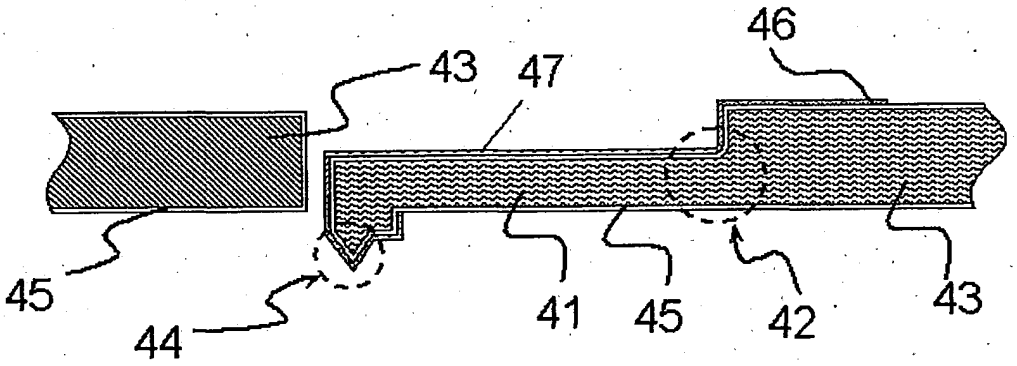


FIG.5C

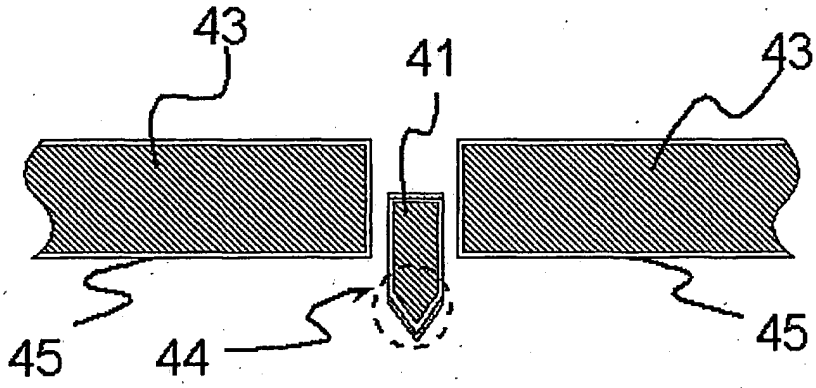


FIG.5D

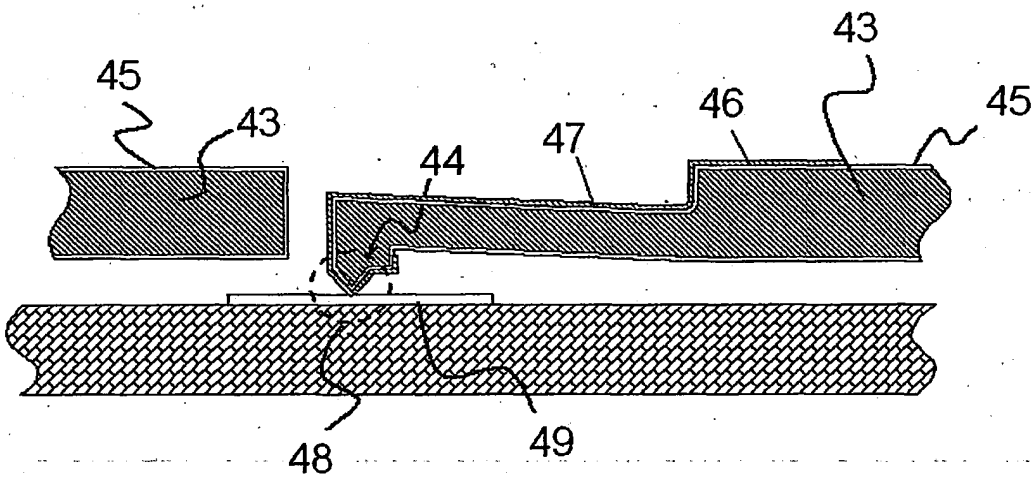


FIG.6A

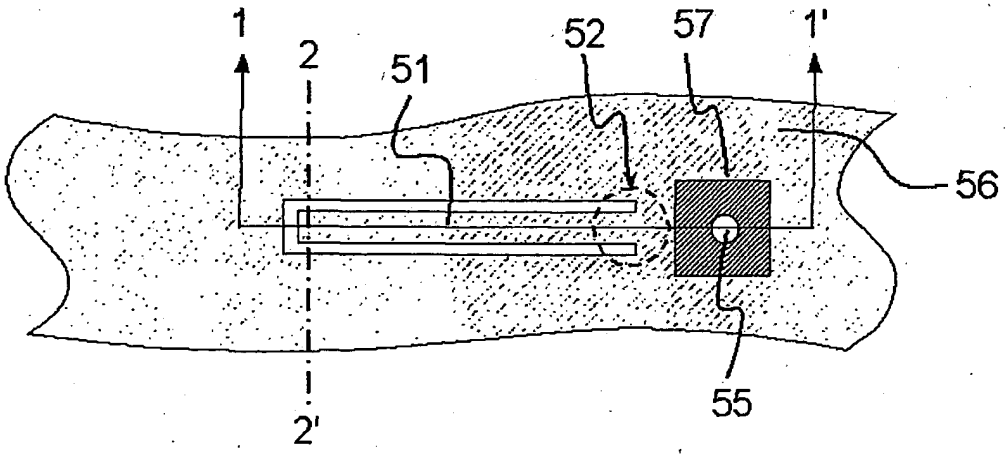


FIG.6B

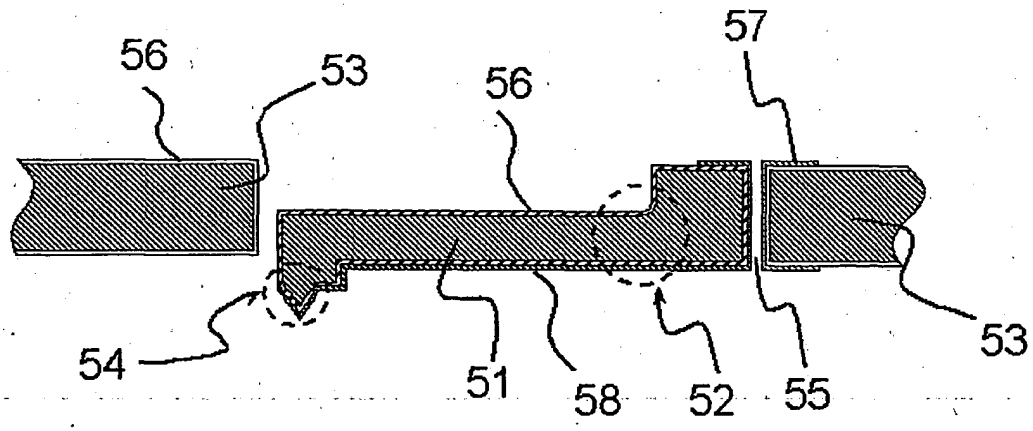


FIG.6C

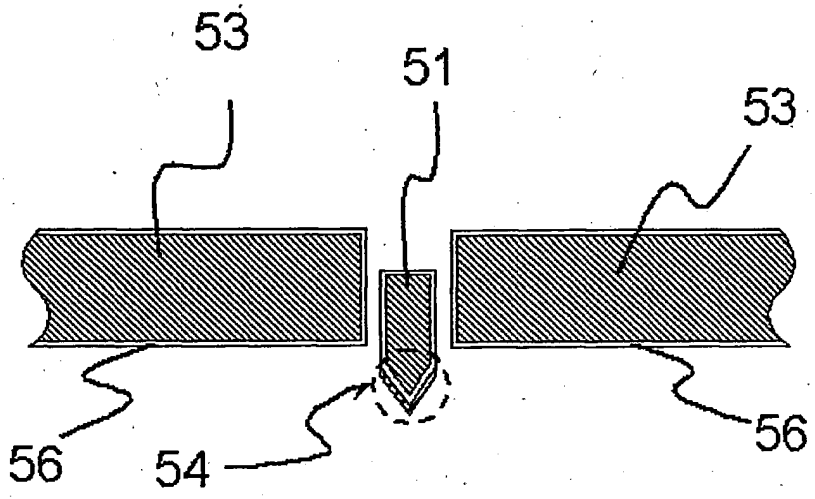


FIG.7A

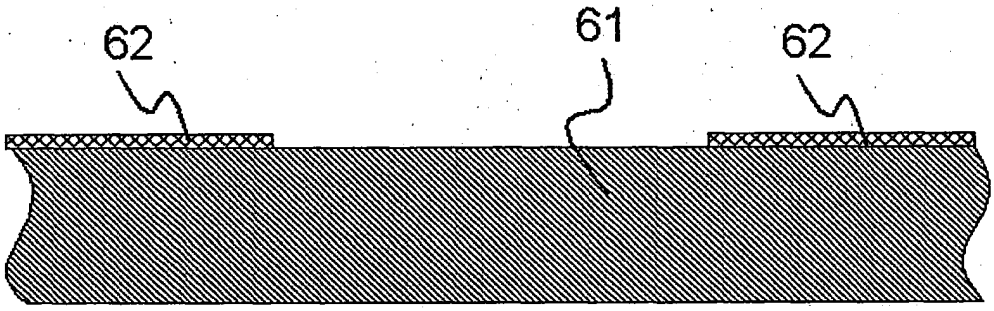


FIG.7B

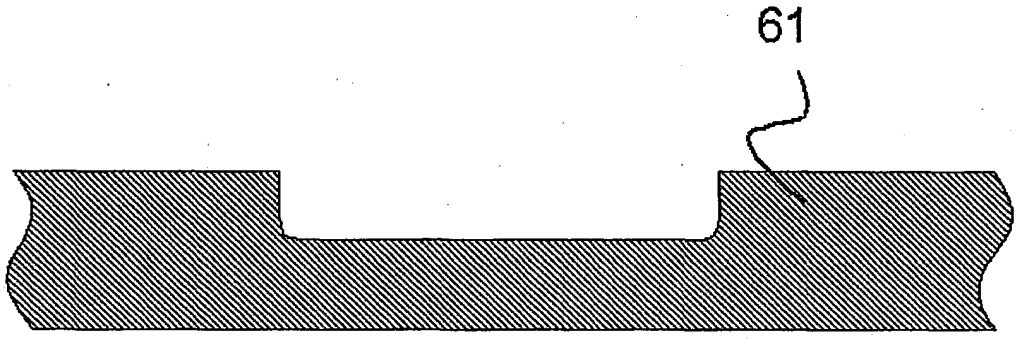


FIG.7C

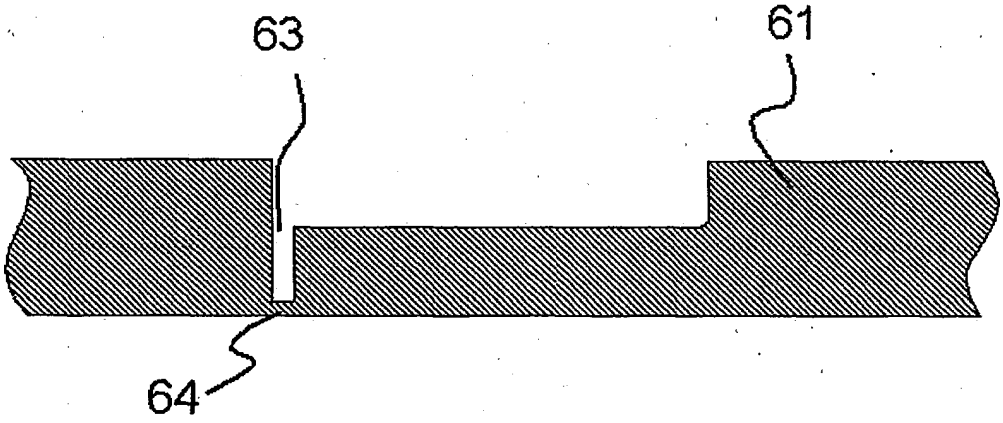


FIG.7D

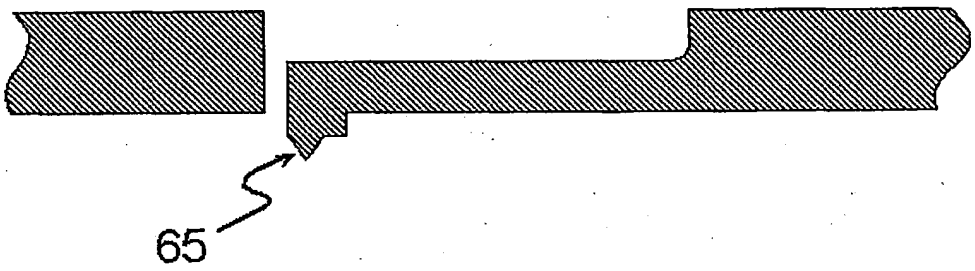


FIG.7E

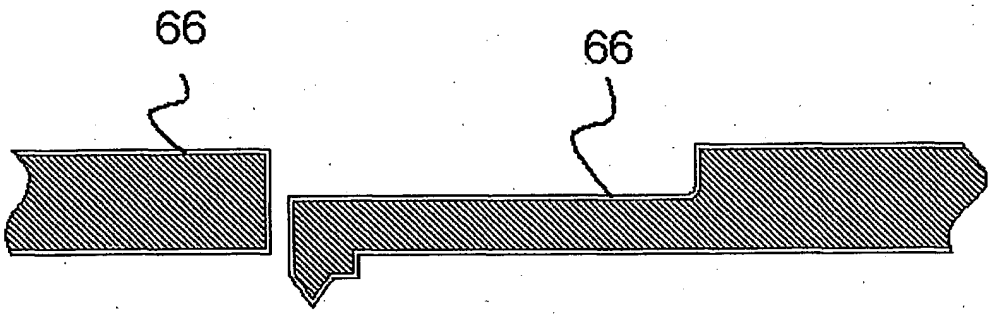


FIG.7F

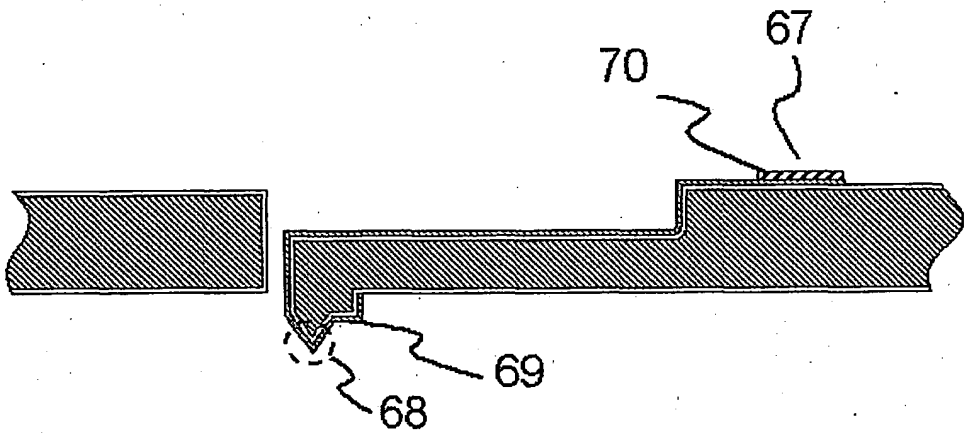


FIG.8A

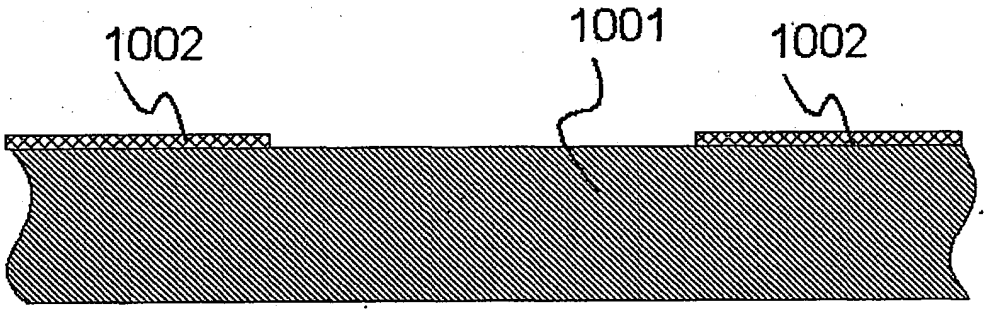


FIG.8B

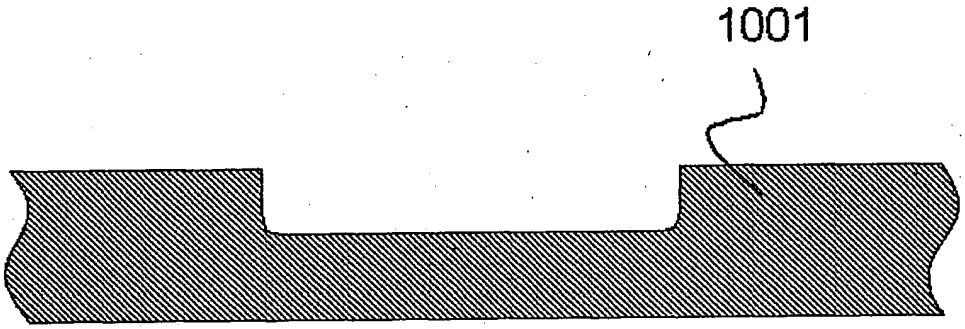


FIG.8C

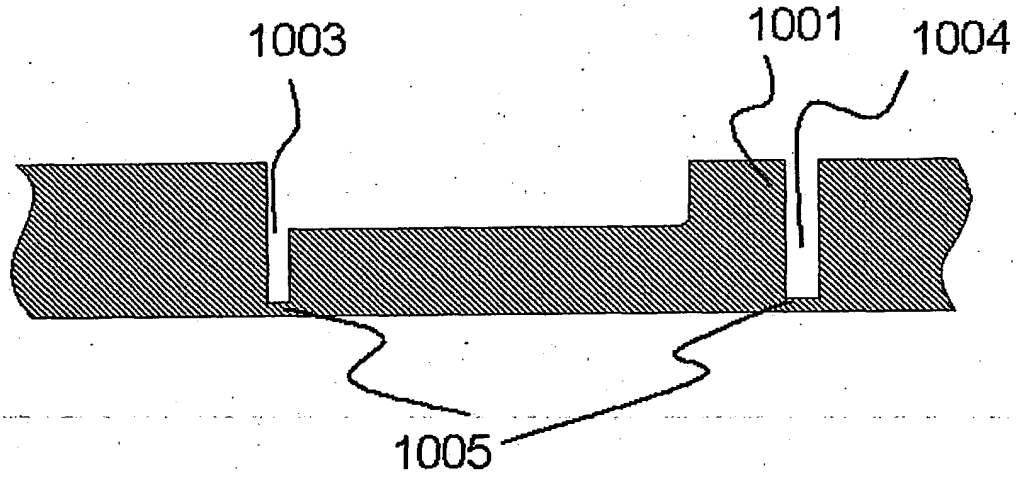


FIG.8D

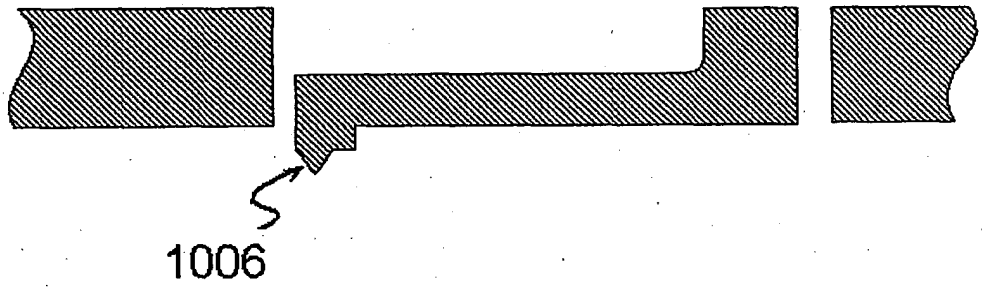


FIG.8E

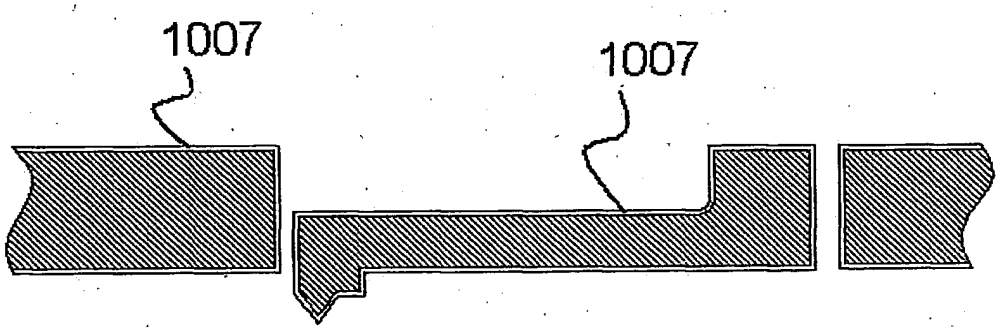


FIG.8F

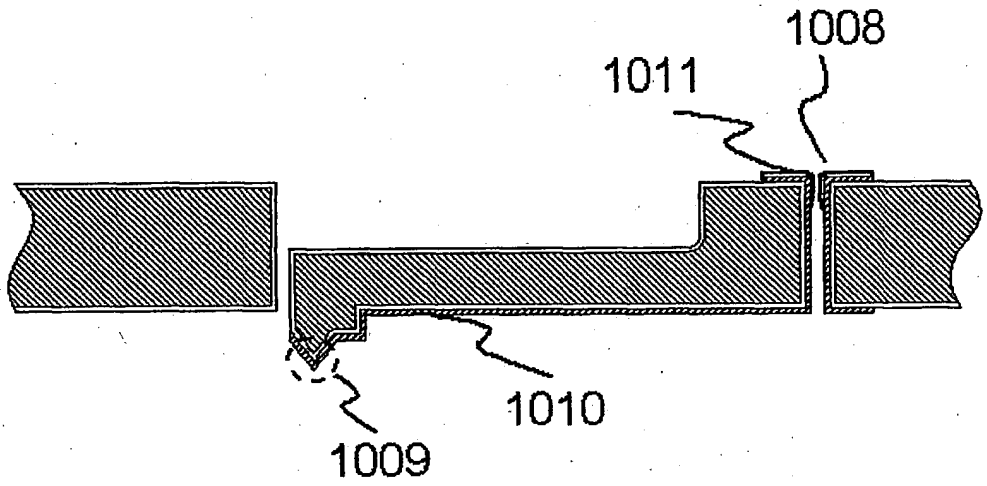


FIG.9

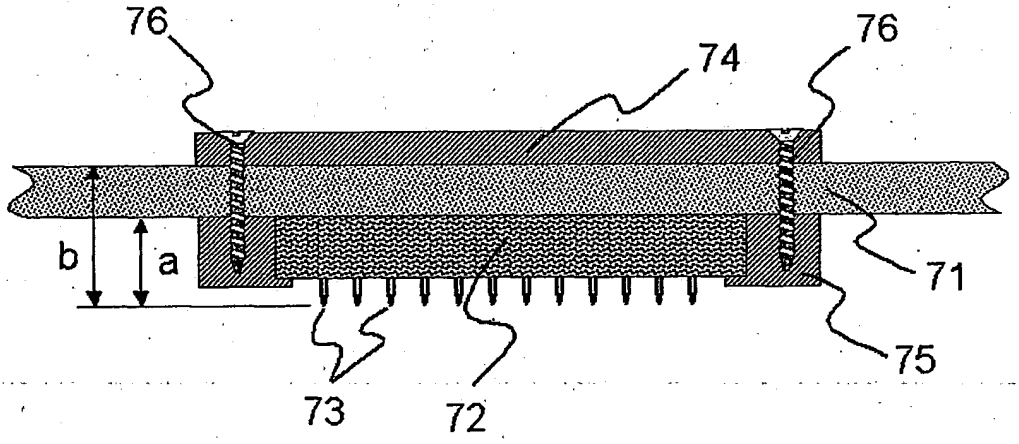


FIG.10

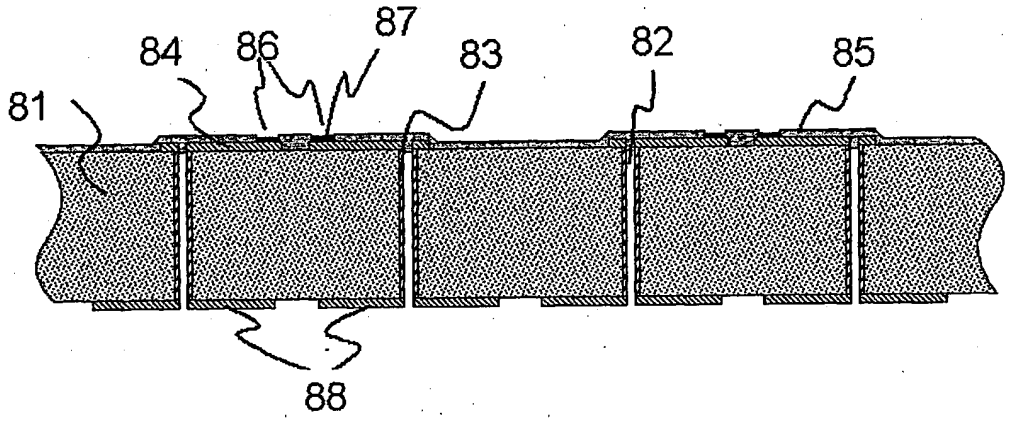


FIG.11A

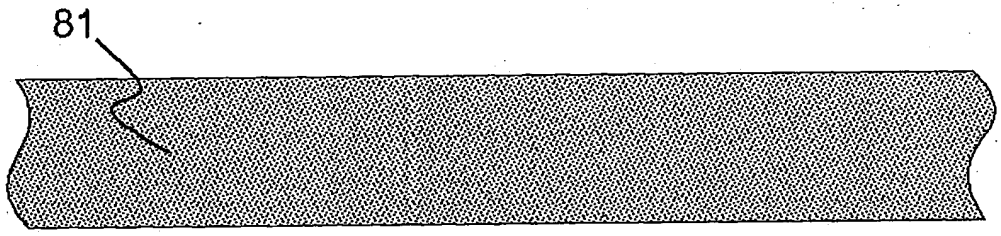


FIG.11B

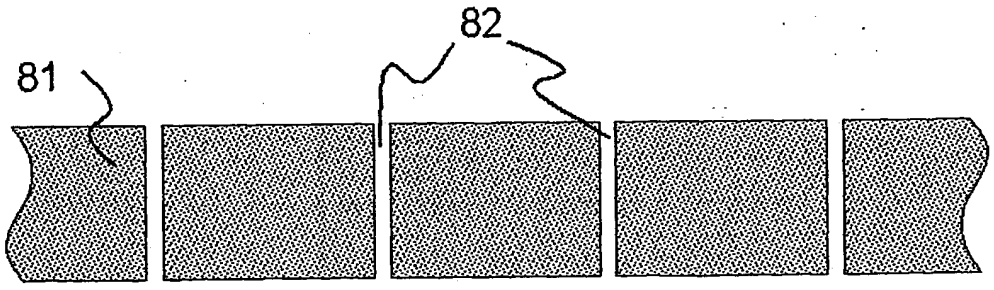


FIG.11C

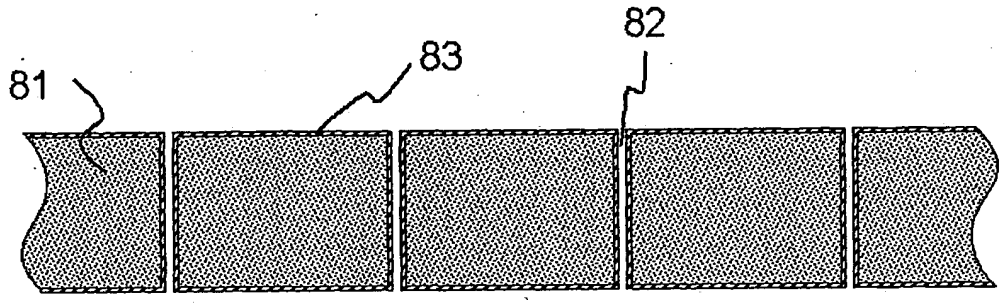


FIG.11D

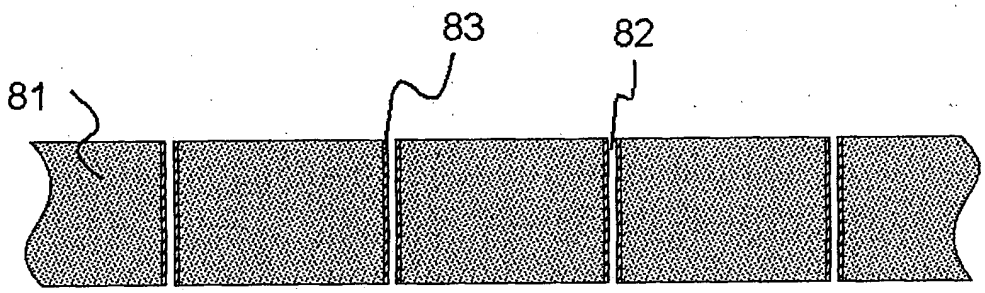


FIG.11E

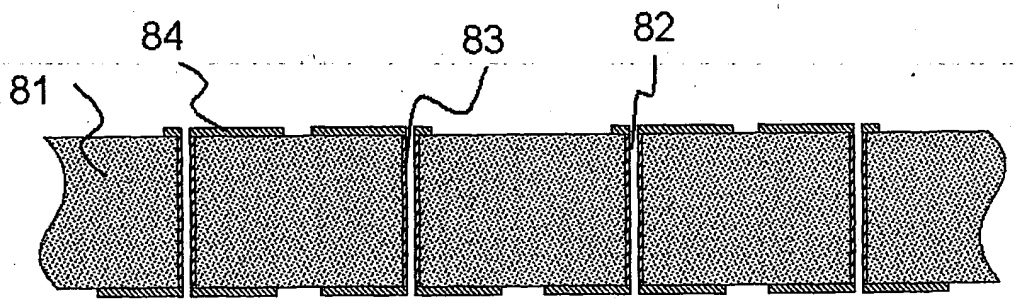


FIG.12A

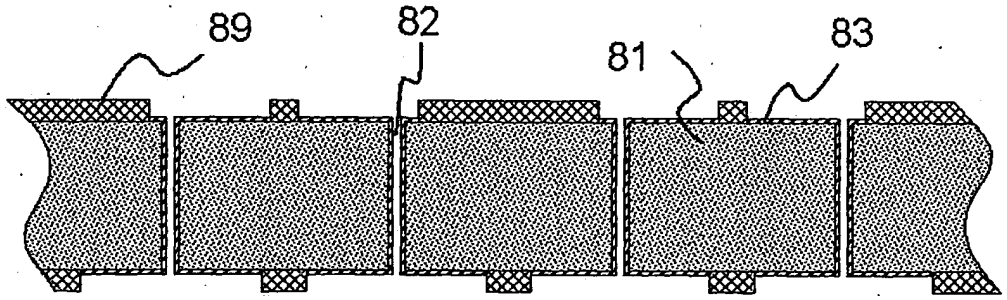


FIG.12B

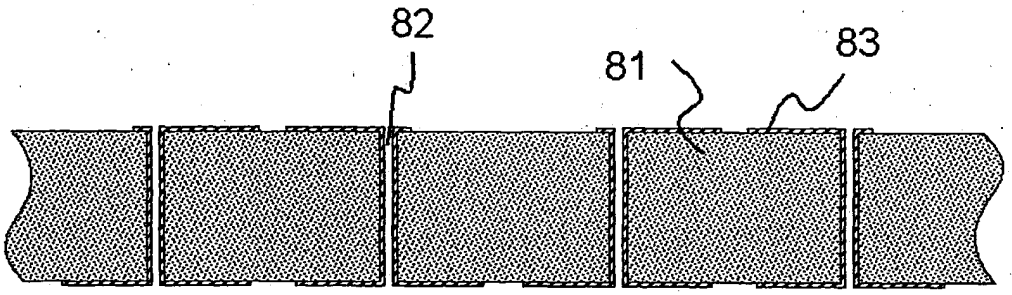


FIG.13

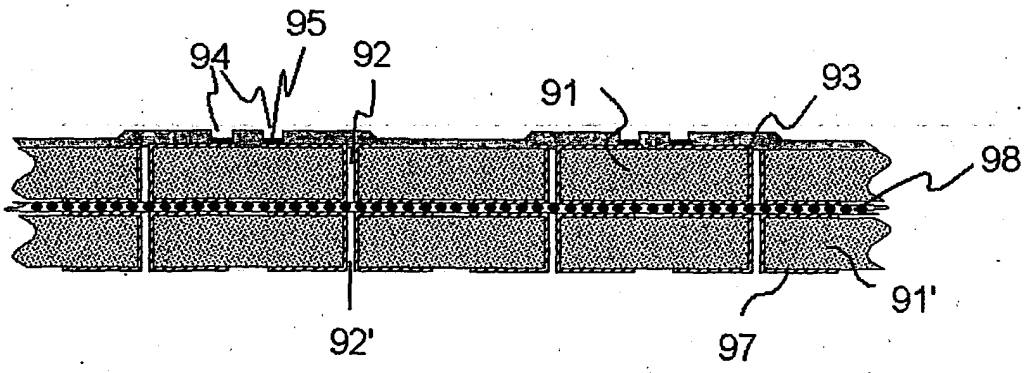


FIG.14A

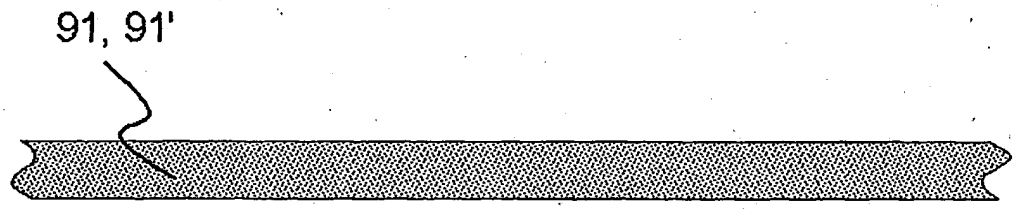


FIG.14B

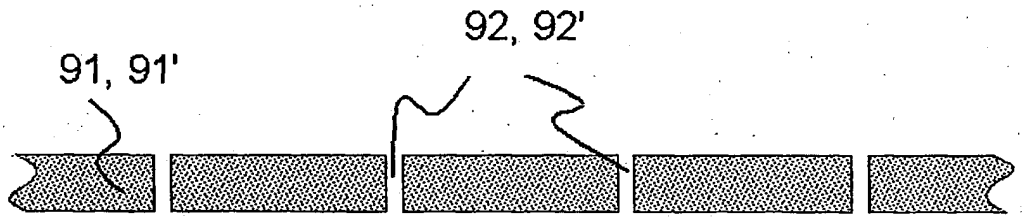


FIG.14C

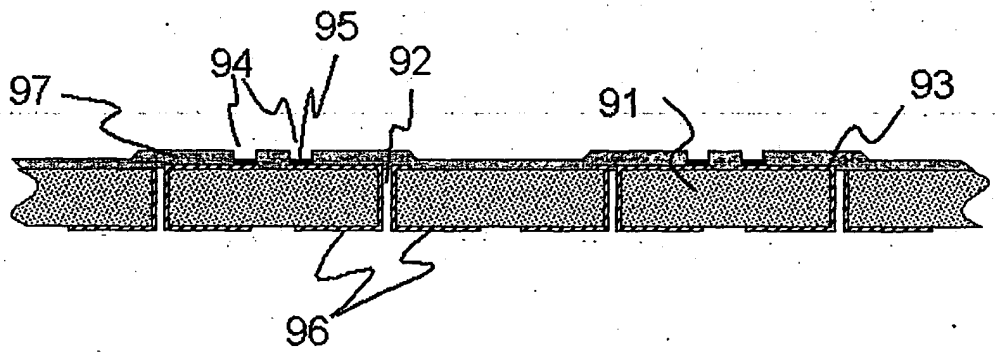


FIG.14D

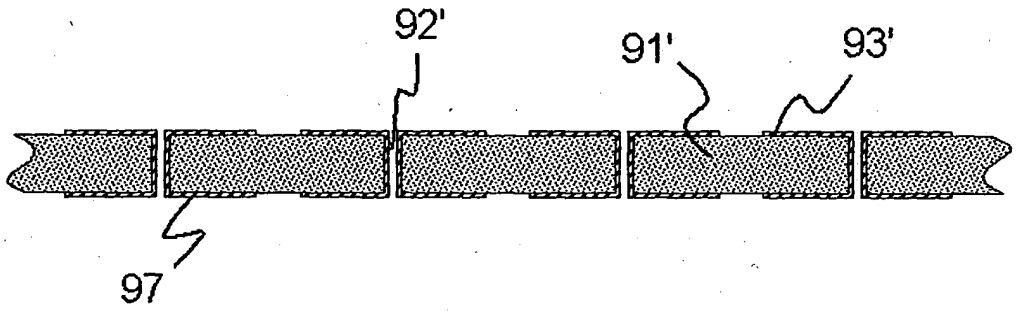


FIG.14E

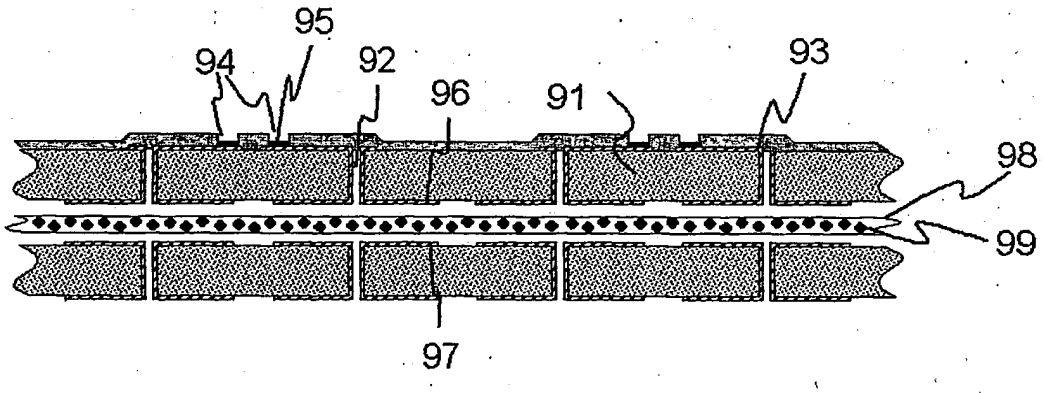


FIG.15A

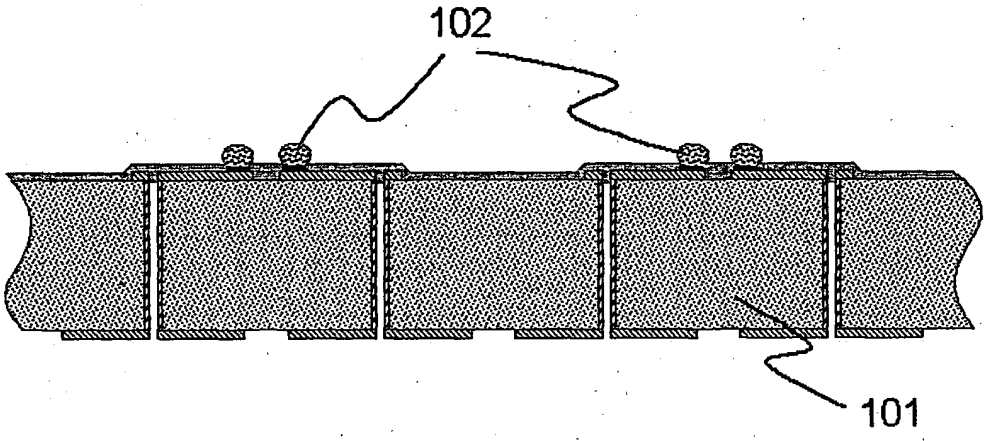
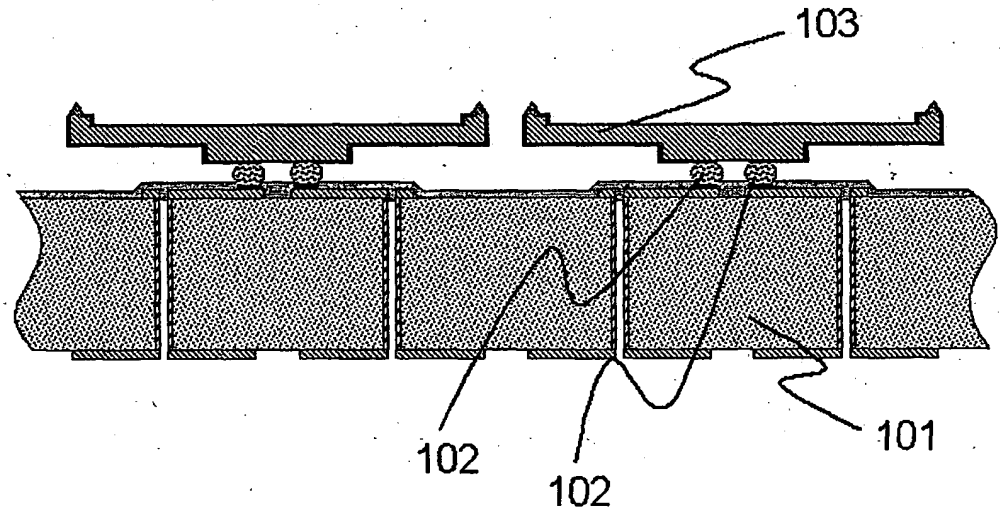


FIG.15B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 01/01358

CLASSIFICATION OF SUBJECT MATTER

IPC[7]: H01L 21/66, G01R 31/303, G01R 1/073

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[7]: H01L, G01R, H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5982183 A (SANO) 9 November 1999 (09.11.99) *figs. 1-8, claims 1-9.*	1-21
A	JP 10 282146 A (NEC) 23 October 1998 (23.10.98) *figs. 1-16, abstract.*	1-21
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P,A	JP 2001 0500983 A (JSR CORP) 23 February 2001 (23.02.01) *figs. 1-33, abstract.*	1-21

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 October 2001 (19.10.2001)	6 December 2001 (06.12.2001)
Name and mailing adress of the ISA/AT Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/535	Authorized officer HEINICH Telephone No. 1/53424/454

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 01/01358

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern[illegible]al application No.
PCT/KR 01/01358

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